Power Efficient Electronic System Design

New design methodologies with energy-delay characteristics that outperform that of the synchronous timing and control approach are needed today because the throughput of systems realized with this method is limited by the power dissipation of nanometer scale devices and the power management strategies developed to insure that they do not exceed device thermal constraints. A circuit timing approach that is not dependent only on the propagation delay of the critical path is required to achieve this for a specified technology and supply voltage. Optimized self-timed circuits have this characteristic and therefore outperform synchronous designs for a given energy dissipation. A novel circuit device sizing approach that is based on the circuit input data distribution is proposed in this paper. The analysis is based on the Logical Effort RC model of a ripple-carry adder. The model was extracted from SPICE simulation for the TMSC 0.18um process. The performance and energy dissipation of circuits implemented with this approach is 7% and 13% respectively better than circuits designed with previously proposed approaches.

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